AND, AT THE WAFER LEVEL

For many in the industry, performing final test at the wafer level is still a novel idea. While providing some much needed solutions, it also comes with its own set of challenges. The four papers in this session look at wafer-level test from a number of different perspectives. The first one discusses the mechanical and electrical differences between wafer-level probe and wafer-level test using spring pins, focusing on requirements for performing final test at the wafer-level. The second presentation provides a comparison between traditional probe test for an RF wafer level chip scale package (WLCSP) and a final test socket solution. TSV issues lead our third author to share technologies that can bridge between 3D stacking and the 3D IC without TSVs. Finally, we'll gain insight into what some consider the holy grail of burn-in and test – wafer-level burn-in (WLBI). Now that WLBI is possible, it's important to understand when it's appropriate to consider WLBI versus other burn-in alternatives.

Spring Probes and Probe Cards for Wafer-Level Test

Jim Brandes—Multitest

A Comparison of Probe Solutions for an RF WLCSP Product

James Migliaccio—RF Micro Devices

This Paper

Bridging Between 3D and 3D TSV Stacking Technologies

Belgacem Haba, Ph.D.—Invensas

Wafer-Level Burn-in Decision Factors

Steve Steps—Aehr Test Systems

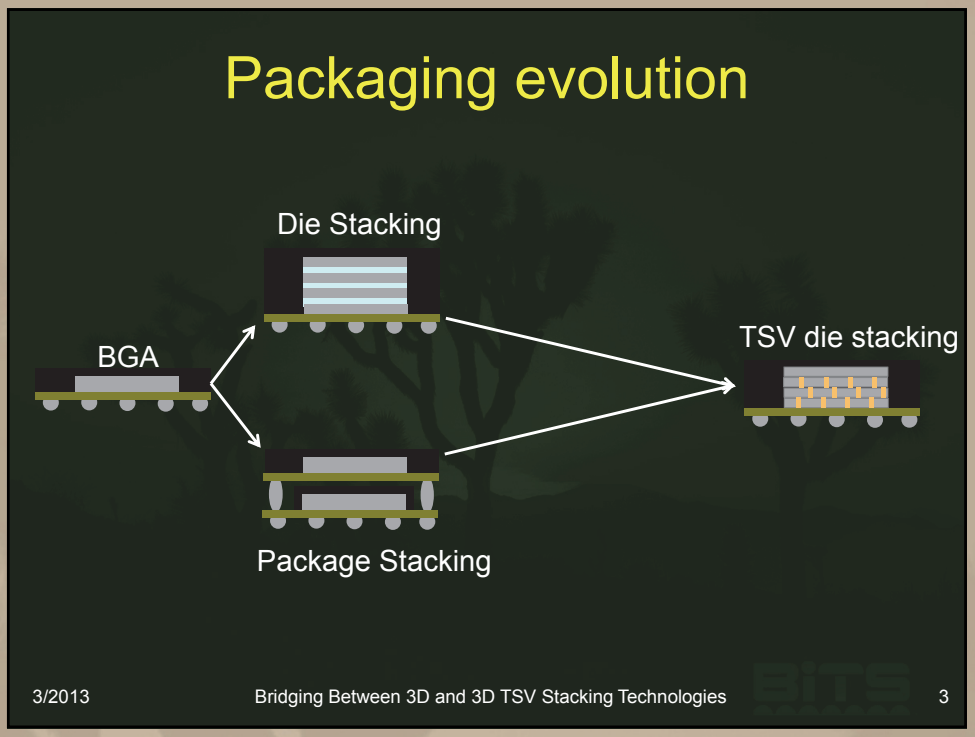
Bridging Between 3D and 3D TSV Stacking Technologies

Belgacem Haba, Ph.D.
Invensas

2013 BiTS Workshop
March 3 - 6, 2013

Content

- Introduction
- DRAM Application
- Package on Package Application
- Summary


Packaging evolution
Die Stacking
BGA
TSV die stacking
Package Stacking
3/2013
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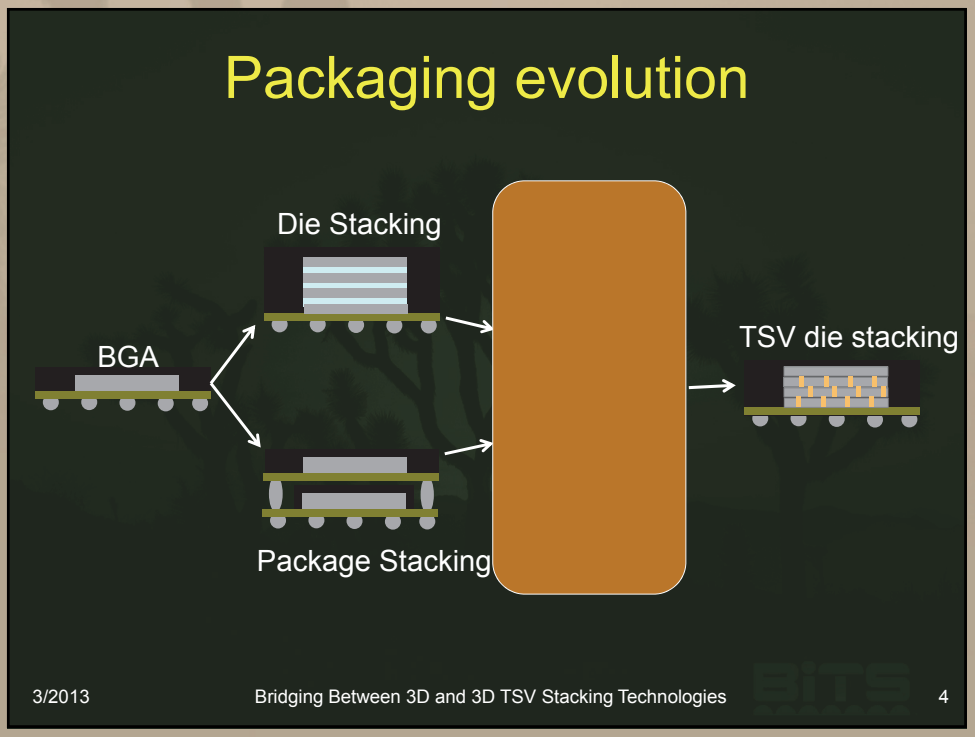
3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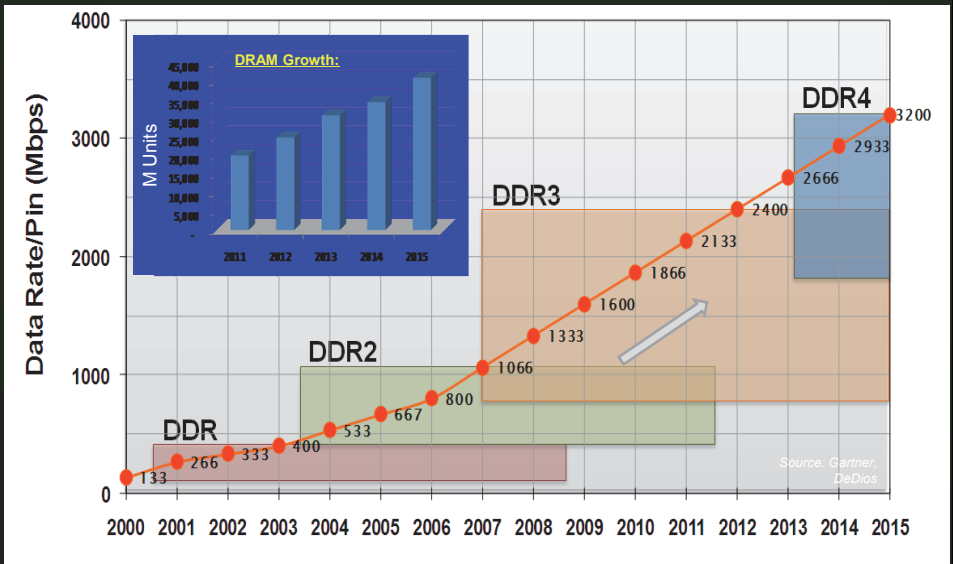
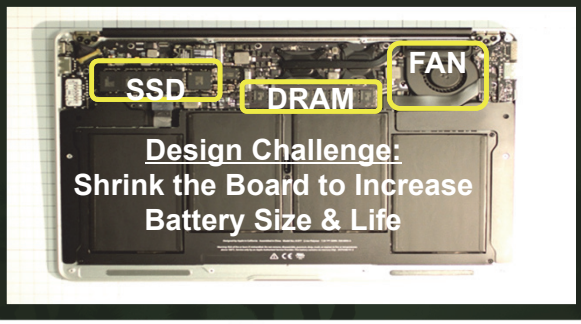
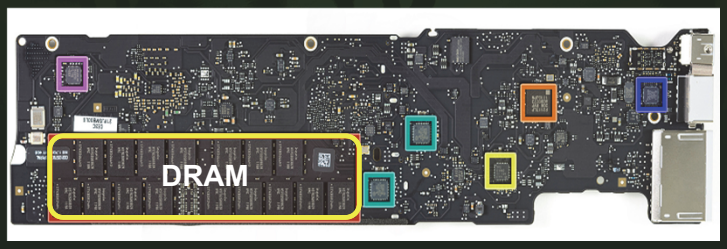
- Summary

DRAM Challenge: 2012-2017



Denser: "Ultra-Book" Memory Form-Factor





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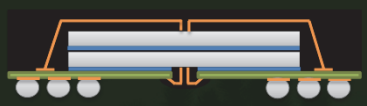
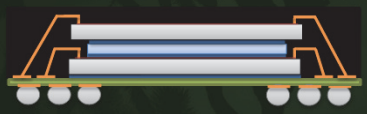
Dual Die DRAM Package Structures



Opposing-Face DDP

Face-Up DDP with FOW



Face-Up DDP with RDL

Dual Face Down (DFD)

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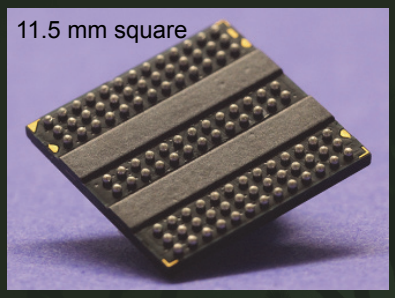
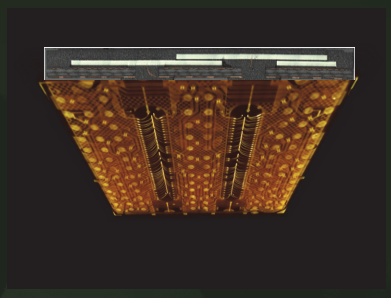
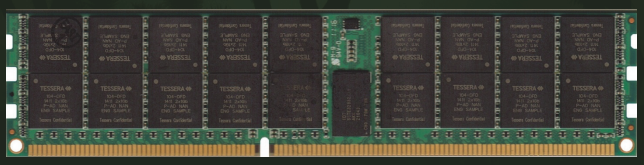
DFD Photos







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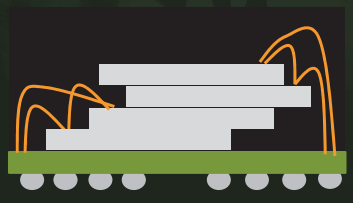
RDL QDP Structures: Spacer and Stairstep

(QDP: Quad Die Package)

RDL QDP (with spacers)



Stair step QDP (no spacers)

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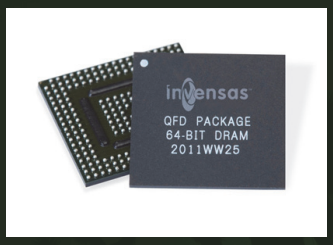
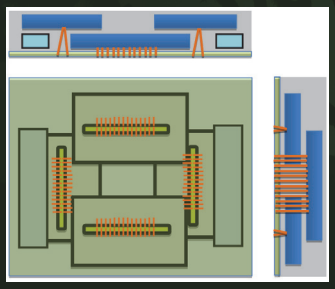
New Quad Die DRAM Package "QFD™"



17 x 17 mm x 1mm tall

Quad Face Down

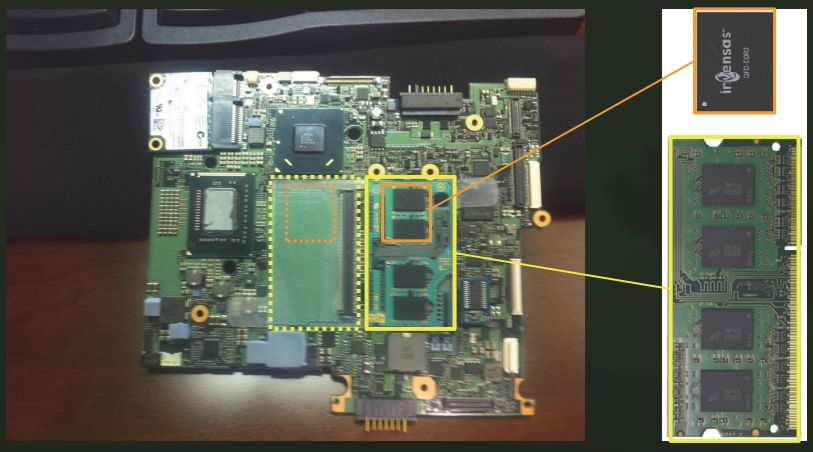


Single-pass Wirebond

Four DRAM die
two spacer die
No RDL,
Short bondwires
Thin construction:
- Two die tall
- No topside wirebonds

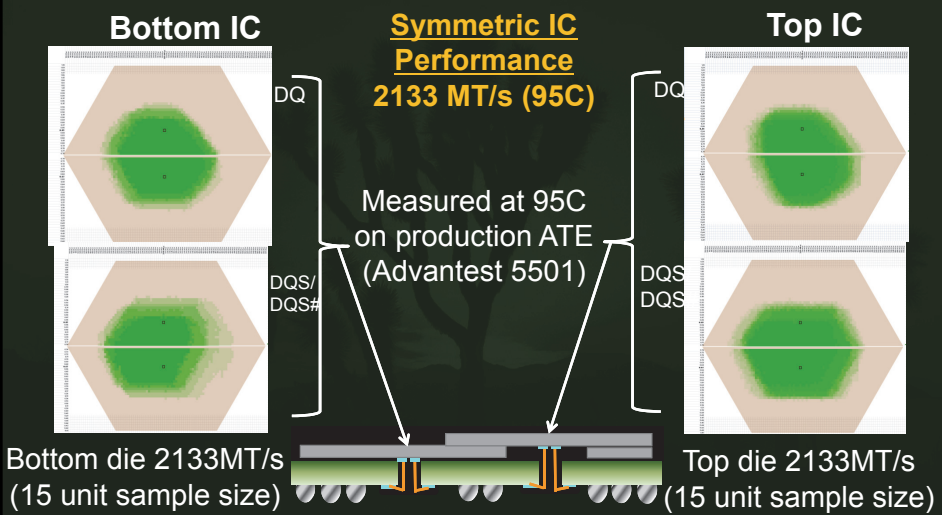
Improved thermal properties

Form factor



Standard SO-DIMM (2,640mm^2) vs.
DIMM-in-a-PACKAGE (394mm^2)

Faster: Monolithic Performance from All Die

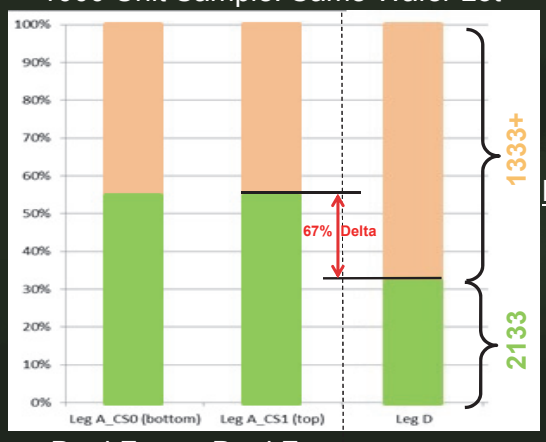


Significant Speed Bin Yield Gain

Speed Bin Yield

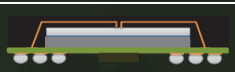
1000 Unit Sample: Same Wafer Lot

DDP = Dual Die Package



Dual Face Down: Bottom Die | Dual Face Down: Top Die | DDP Control

DDP Control Structure

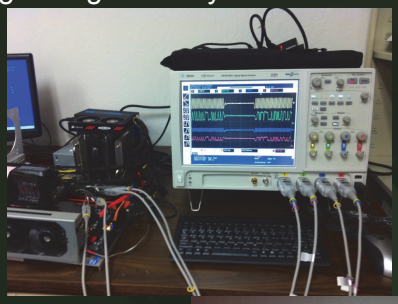


Dual Face Down Structure

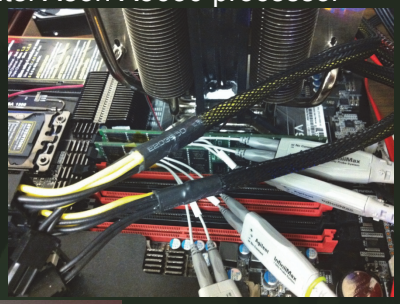
67% gain in 2133MT/s speed bin yield vs. control DDP using same wafer lot.

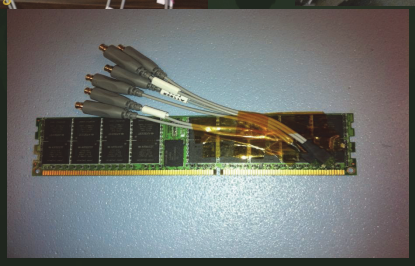
In-System Test Setup

Agilent Infinium DSA91204A 12GHz Digital Signal Analyzer



EVGA SR-2 Classified motherboard Intel Xeon X5650 processor





For full-speed in-system probing of DQ, DQS

Functional At-Speed Testing DFD

Module Tested	Component Nominal Speed Die density & # die/module	One DIMM/Channel (4 DQ loads/channel)	Two DIMMs/Channel (8 DQ loads/channel)
Invensas 8Gbyte Quadrank RDIMM w/DFD (1Gbit (x4)) die)	1333 MHz Components 1Gbit (x4 org x 2/package) (72 memory die/module)	>1600MT/s	1600MT/s
Market 8Gbyte Quadrank RDIMM with single die packages (2Gb: single x8 die)	1333 MHz components 2Gbit (x8 org x 1/package) (36 memory die/module)	~1600MT/s	800MT/s (barely operates)
Market 16Gbyte Quadrank RDIMM with DDP packaging (2Gb: x4 die, DDPs)	1333 MHz components 2Gbit (x4 org x 2/package) (72 memory die/module)	~1600 MT/s	800MT/s (barely operates)

DFD Reads DIMM1&2, 2DPC, 1600MT/s

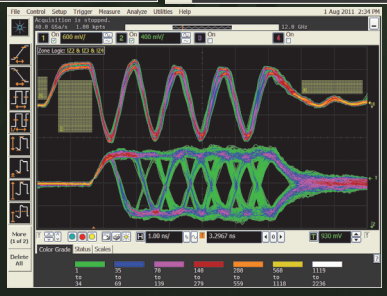
DQS (DIMM0)

DQ1 (DIMM0)

DQS (DIMM1)

DQ1 (DIMM1)

DIMM0 being read



DIMM1 being read

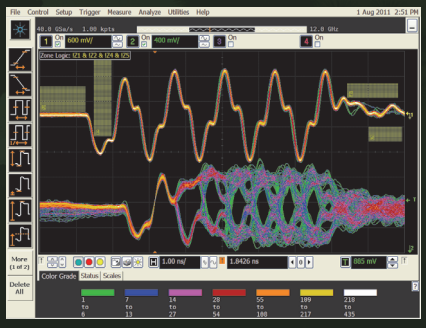
DFD Writes at 1600MT/s and 2DPC

DQS (DIMM0)

DQ1 (DIMM0)

DQS (DIMM1)

DQ1 (DIMM1)



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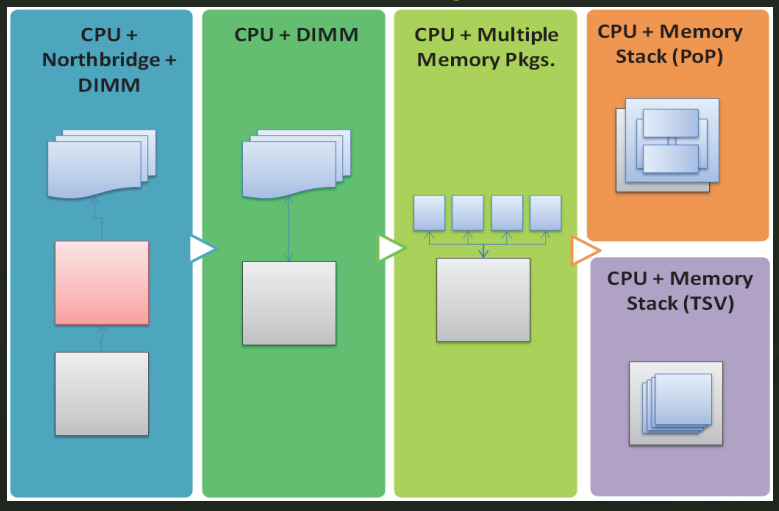
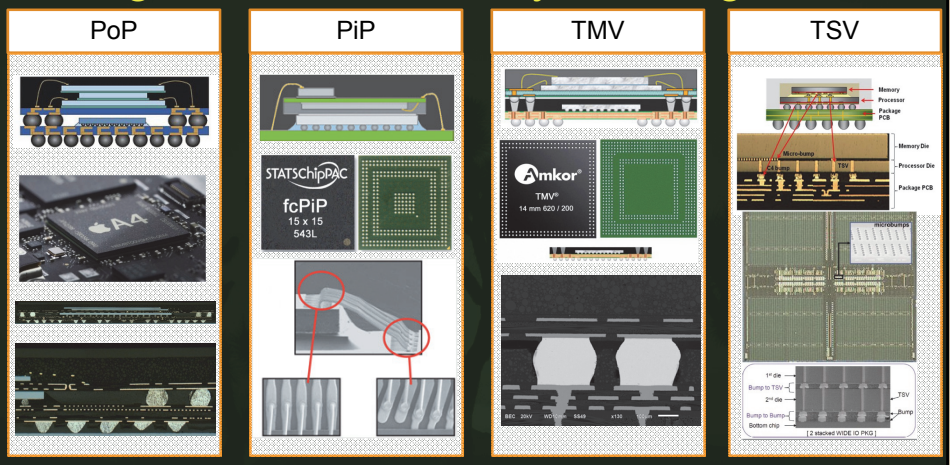
Processor-Memory Architecture



The interconnect determines the computing performance and power usage

Existing Processor-Memory Stacking Solutions



- The total market size for Package-on-Package stack was about 800M in 2010
- Except for TSV, the stack packaging infrastructure is well established

Wide IO Roadmap

	2010	2011	2012	2013	2014	2015	2016?
Mobile DRAM	LPDDR		LPDDR2	LPDDR3 Emerging			Wide IO
Packaging	PoP	PoP	PoP	PoP			TSV
Mobile processor to memory interconnect	168	168	240	240			1250
Clock Speed (MHz)	400		533	800			200
Power	2X		1X	0.8X			0.5X
# of Channels	Single	Single	Dual	Dual			Quad+
Bandwidth (GBps)	1.6	4.2	8.5	12.8			>12.8

- Wide IO is approximately an order of magnitude increase in IO compared to current memory interface
- One method of implementing wide IO is using memory with TSV, which is not expected within the next few years

Wide IO Roadmap

	2010	2011	2012	2013	2014	2015	2016?
Mobile DRAM	LPDDR		LPDDR2		LPDDR3 Emerging	Wide IO	Wide IO
Packaging	PoP	PoP	PoP	PoP	BVA PoP		TSV
Mobile processor to memory interconnect	168	168	240	240	IO ranging from 200 to 1000+		1250
Clock Speed (MHz)	400		533	800	High IO offers high bandwidth at low speed		200
Power	2X		1X	0.8X	Enables intermediate power reductions		0.5X
# of Channels	Single	Single	Dual	Dual	Quad+		Quad+
Bandwidth (GBps)	1.6	4.2	8.5	12.8	>12.8		>12.8

- The goal of BVA PoP is to offer TSV capabilities for PoP applications utilizing conventional PoP infrastructure and materials

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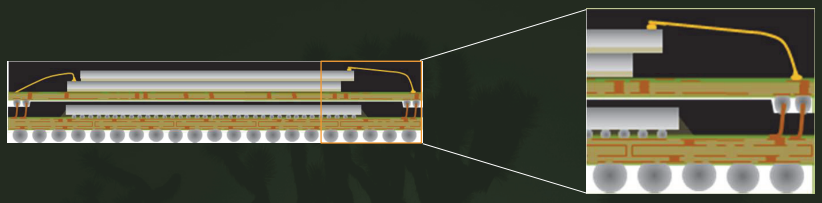
BVA



- Stand-off issue eliminated: Wire-bond based memory-logic interconnect
- 1000+ wide IO: 0.2 mm pitch easily possible
- High performance at low-cost: Conventional PoP materials and processes

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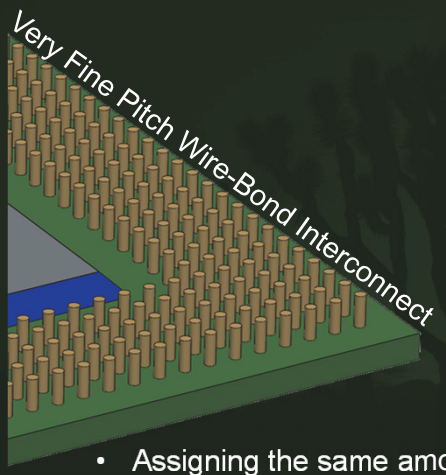
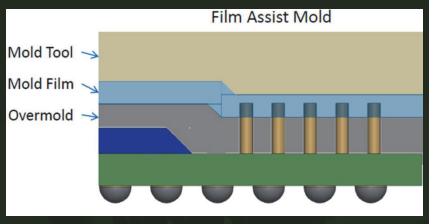
BVA PoP Scalability



Pitch (mm)	No. of IO rows				
	2	3	4	5	6
0.50	200	288	-	-	-
0.40	248	360	-	-	-
0.30	336	492	640	-	-
0.25	408	600	784	960	-
0.20	512	756	992	1220	1440

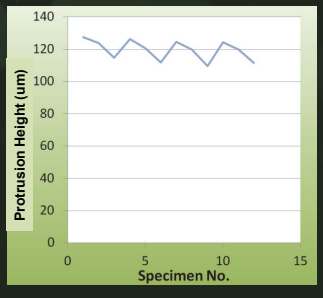
- Assigning the same amount of area for IO as that of the current 0.5 mm pitch PoP, BVA with 0.2 mm pitch can offer up to 1440 IO

Overmold and Wire Exposure Process



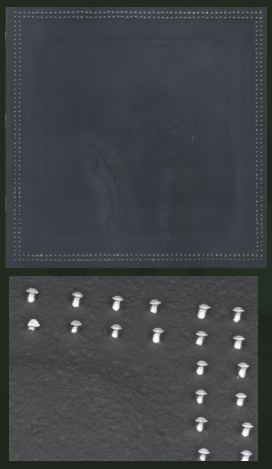
Top view of Overmolded bottom package

Average wire protrusion height

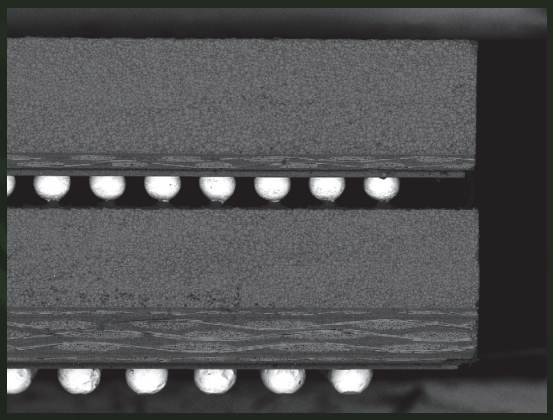


Test Vehicle Assembly: PoP Stack

Top surface of bottom package



Fully Assembled BVA PoP Package



- The top surface of the of the bottom package has bond wires projecting outwards by about 0.1 mm. The two packages were joined using conventional PoP SMT approach

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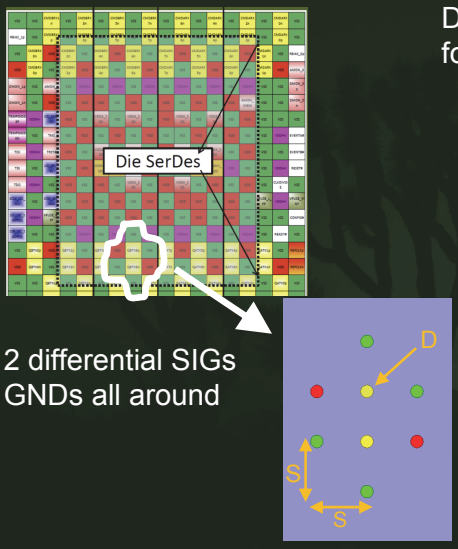
Differential impedance



2 differential SIGs
GNDs all around

Different technology implementation for target impedance

Dbva (um)	S (um)	Differential Impedance (ohm)
50	240	125
50	280	135
50	320	144
50	360	151
50	400	158

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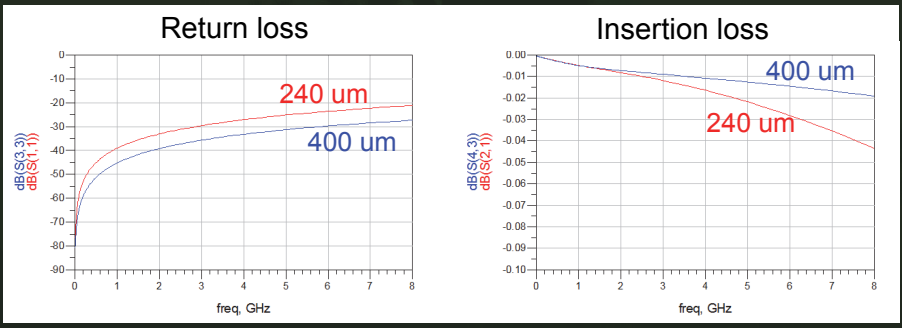
Differential return loss and insertion loss

Dbva (um)	S (um)
50	240
50	400



BVA itself is not too big an issue for RL and IL – assumed 550 um BVA height

Summary

- Demonstrated two technologies that can bridge the gap before the TSV technology arrives
- The two technologies offer platforms for higher bandwidth
- Platforms that uses available assembly and available testing infrastructures