STREAMLINING OPERATIONS

Test operations, generally considered costly, yet necessary, add value to device manufacturing when optimized for efficiency. This session offers a variety of approaches that promise high yields, lean manufacturing, maximized performance at minimal costs, and optimized production times. The first paper discusses a method of incorporating multidimensional Monte Carlo analysis simulation with known design parameters to focus manufacturing improvement efforts and maximize alignment performance while minimizing costs. Presented next is a method for redefining test tooling design rules to gain process margin and prevent substrate chipping caused by test handler misalignment. Zero-cost, software based, virtual tool checkers that bring the whole production area towards a manufacturing LEAN direction is then discussed. Wrapping things up is a paper on a screwless socket and dual pin testing concept said to greatly enhance the robustness and efficiency of IC testing.

Improving Socket Alignment Performance Using Monte Carlo Analysis Techniques and Manufacturing Controls

Daniel DelVecchio, Dustin Allison—Interconnect Devices Incorporated

Tooling Stack-up Process Margin Improvement

Mook Koon Wong, Boon Hor Phee—Intel Malaysia

This Paper

Zero Cost Virtual Tool Checker

Seong Guan Ooi—Intel Technology Sdn. Bhd.

Enablers for Robust & Fast Online Trouble-shooting for High Parallelism Testing

Benedict Loh—Infineon Technologies
Kohei Hironaka—NHK Spring Co. Ltd.
Michelle Ng—TestPro

Zero Cost Virtual Tool Checker

Seong Guan Ooi
Intel Technology Sdn Bhd

2013 BiTS Workshop
March 3 - 6, 2013

Content

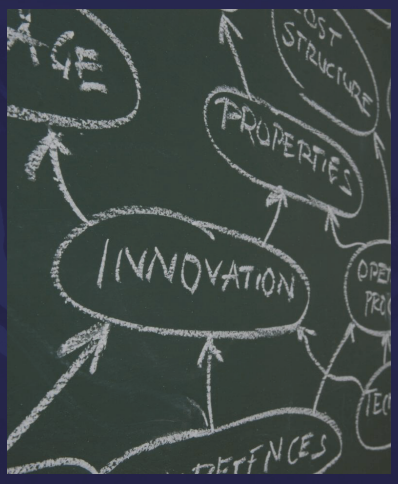
- Problem statement
- Project Concept & Algorithm
- Project Application
- Results & Data Interpretation
- Summary
- Acknowledgement

Problem Statement

- Challenges in equipment troubleshooting today
  - **Reactive** - Solve problem when problem happen.
  - **Time consuming** – To identify problem root cause in a complex test cell.
  - **Unpredictable** – Lack of real time in-depth test cell health tracking system.
  - **System Complexity** – Problem might consists of tester, handler, load board, docking, pogo pins, socket, etc.
  - **Human dependency** – In-depth test methodology knowledge and troubleshooting experience required.

No standard method to resolve a day to day production issue.

Project Concept & Algorithm



Project Concept & Algorithm

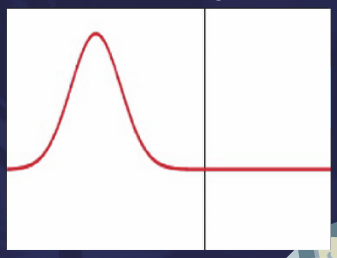
- Theory & Concept
  - Gain, Offset & Time Domain Reflectometry (TDR)
- Project Algorithm Overview
- Calibration
  - Type of ATE calibration
  - Calibration file content
  - Calibration file handling
- Statistical Analysis Software (JMP)
- Scheduler email system

Theory & Concept

- Gain
  - A measure of the ability of a circuit to increase the power or amplitude of a signal from the input to the output, by adding energy to the signal.
  - Voltage Gain $V_{Gain} = 20\log\left(\frac{V_{out}}{V_{in}}\right)dB$
  - Current Gain $I_{Gain} = 20\log\left(\frac{I_{out}}{I_{in}}\right)dB$
- Offset
  - Imbalances of a result signal

Theory & Concept

- Time Domain Reflectometry (TDR)
  - A measurement technique used to determine the characteristics of electrical lines by observing reflected waveforms.
  - Checking criteria:
    - Magnitude
    - Duration
    - Shape of the waveform.



Gain + Offset + TDR = BIN 1

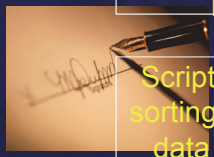
~1

03/2013 Zero Cost Virtual Tool Checker 7

Project Flow Overview

START

Tester generate load board calibration file while loading test program



Script perform data sorting and send raw data file to server

Script get data from server and perform analysis task

Auto email send analyzed data to stakeholders

Stakeholders perform investigate triggered signals

END

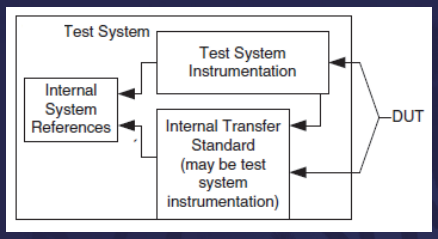
03/2013 Zero Cost Virtual Tool Checker 8

Type of ATE Calibration

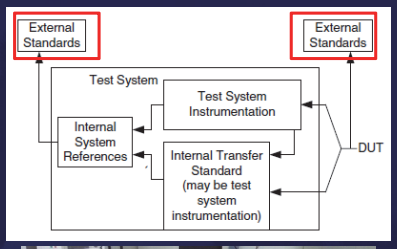
	External Reference Calibration	Internal Reference Calibration	Load Board Calibration
Accessible	User	Test system	Test system
Calibration Equipment Require	• HP53151A frequency counter • HP3458A digital voltmeter (DVM)	• System reference clock • System DC reference board	• Load board • Tester
Purpose	Measure and adjust internal system reference, using traceable external equipment.	Adjust system instrumentation precision via internal standards.	Adjust signal path losses from load board to device under test (DUT) via internal standards.
Calibration Frequency	Monthly, quarterly, semi-annual or annual	• Loading test program • Within a fix time interval based on spec	• Loading new test program. • Condition parameter change

Type of ATE Calibration

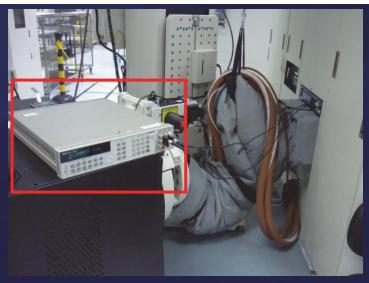
Internal Calibration



External Calibration

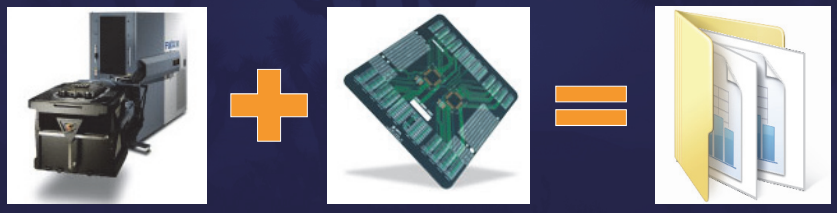



```
Calibrating Voltmeter
Calibrating Source 1
Calibrating Source 2
Calibrating Source 3
Calibrating Source 4
Calibrating DUT Source 1
Calibrating DUT Source 5
Calibrating DUT Source 6
Calibrating DUT Source 7
Calibrating DUT HCU 2
Calibrating DUT HCU 3
Calibrating DUT HCU 4
Calibration Complete
...starting vhfawg #1 calibration
...starting vhfawg Z-cal check
...starting vhfawg detector drift check
...starting vhfawg DC drift check
...starting vhfawg VCA drift check
...starting vhfawg VCA cal
...starting awglan ppmu calibration
...vhfawg #1 calibration passed
```



Load Board Calibration

- Load board calibration
  - Generated by tester while loading test program
  - Compensate channel losses through transmission lines
  - Stored under a specific location at tester workstation for reference purposes



Tester + Load board = Calibration files

Calibration File Content

- Uniqueness of calibration files are:
  - File name constructed from test program & load board ID
  - Consist of instrument channels compensation data used for test
  - Data stored are up to board serial number level

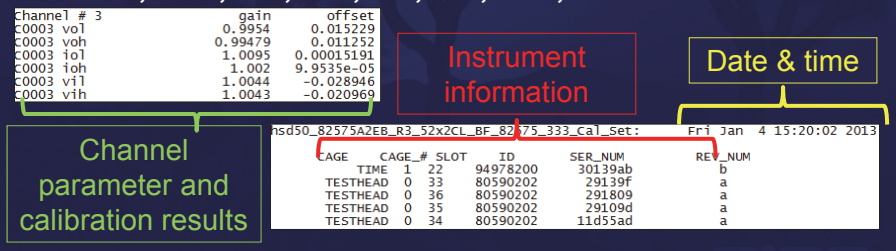
Calibration file path

```
/export/home/pgtig05/image.svr4/tester/pgtig05-t/cal
pgtig05% ls hsd50_8*
hsd50_82575A2EB_R3_52x2CL_BF_82575_301_Cal_Set_h1_cal_11.log.Z
hsd50_82575A2EB_R3_52x2CL_BF_82575_302_Cal_Set_h1_cal_11.log.Z
hsd50_82575A2EB_R3_52x2QA_BF_82575_302_Cal_Set_h1_cal_11.log.Z
hsd50_82576A1EB_Only_R2_7x2CL_BF_82576_036_Cal_Set_h1_cal_11.log.Z
hsd50_82576A1EB_Only_R2_7x2CL_BF_82576_041_Cal_Set_h1_cal_11.log.Z
hsd50_82576A1EB_Only_R2_7x2CL_BF_82576_045_Cal_Set_h1_cal_11.log.Z
```

Type | Test program name | Load board ID | Compressed

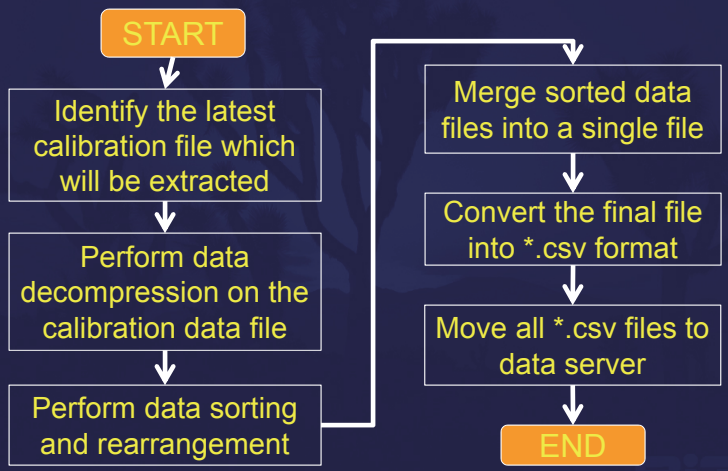
Calibration File Content

- A new calibration file will be generated when:
  - No previous calibration data file found in tester workstation
  - Change in load board or tester instrument
  - Change in tester environmental temperature (+/- 3°C)
  - Validation period expired (1 year)
- Calibration file consists test parameters such as:
  - VOL, VOH, IOL, IOH, VIL, VIH, TDR, etc.



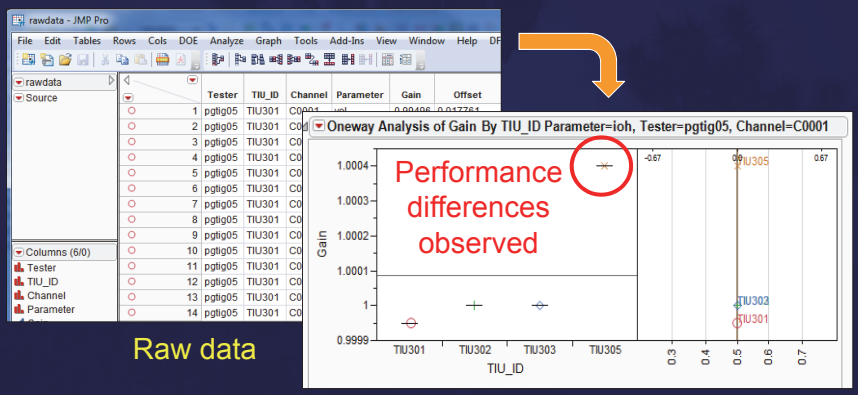
Calibration File Handling

- UNIX shell script was developed to help on calibration data extraction from tester computer to server.



Statistical Analysis Software

- JMP was used to perform data analysis on the extracted data which is stored inside data server along with a customized JMP script.

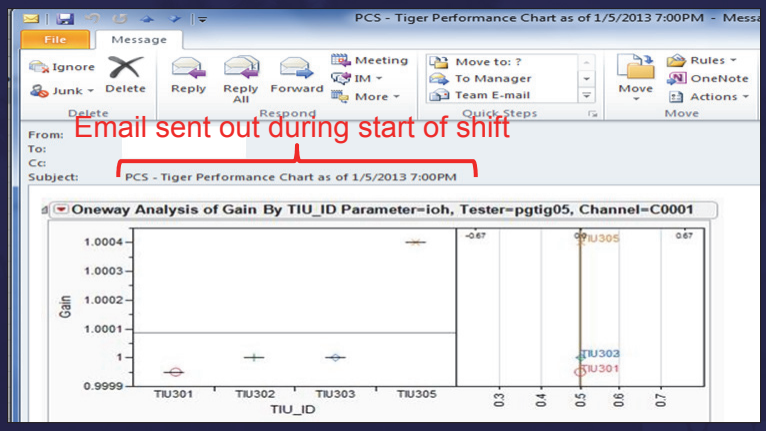


Raw data

Analysis results

Scheduler Email System

- Scheduler email system was setup to distribute JMP analysis results to all stakeholders in a routine manner.



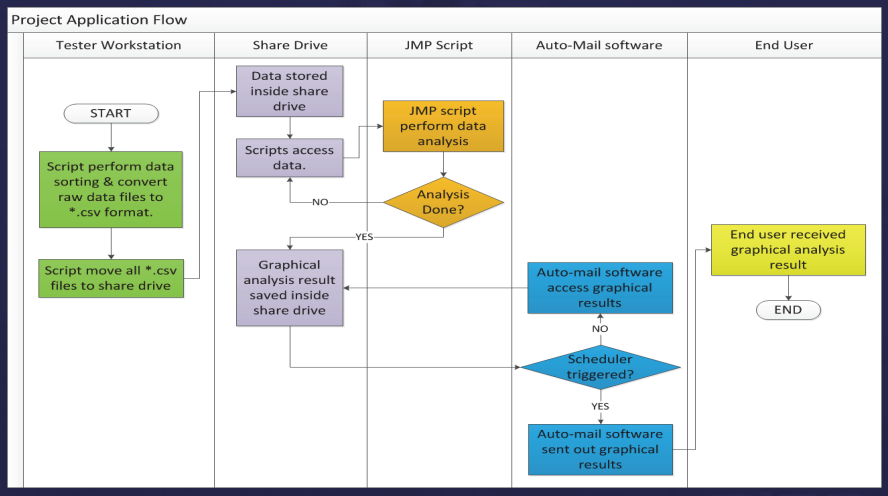
Project Application

Project Application

- Applicable to Unix & Windows based ATE which perform load board calibration while loading test program.
- Up to channel level parametric comparison with reference to tester or load board (user defined).
- Simple setup procedures:
  - Develop Unix script for raw data processing
  - Develop data analysis script & determine key parameters for monitoring
  - Setup scheduler email system and share drive access
- Stakeholders receive scheduler email and perform investigation based on outlier triggers – marginal tools.

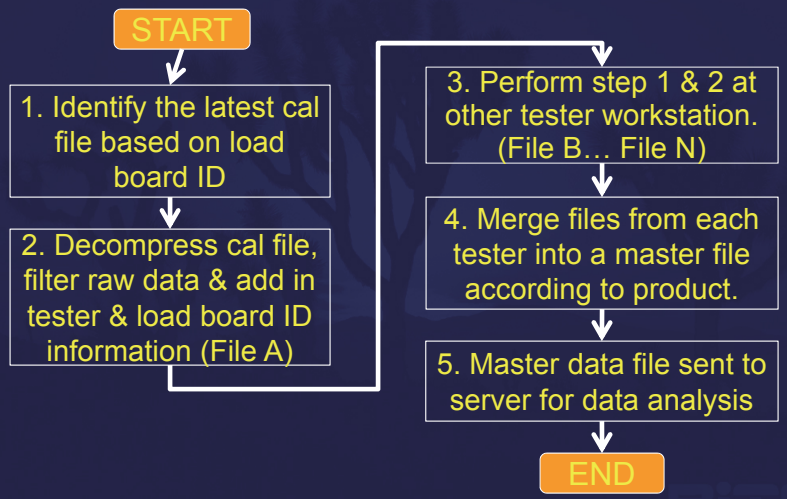
Project Application

- Overall project application flow are shown as below:

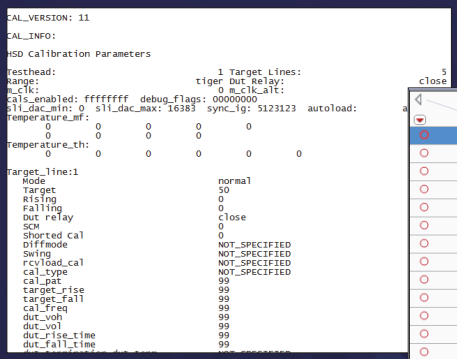


Raw Data Processing

- Raw data processing stages (Tester workstation)



Raw Data Processing



```
CAL_VERSION: 11

CAL_INFO:

HSD Calibration Parameters

Testhead:                          1 Target_Lines:                    5
Xange:                           tiger Dut_Relay:                 close
m_clk:                                0 m_clk_alt:
cals_enabled: ffffffff  debug_flags: 00000000
sli_dac_min: 0  sli_dac_max: 16383  sync_ig: 5123123  autoload:
Temperature_mf:
       0         0         0         0         0
       0         0         0         0
Temperature_th:
       0         0         0         0         0         0

Target_line:1
   Mode                            normal
   Target                          50
   Rising                          0
   Falling                         0
   Dut relay                       close
   SCM                             0
   Shorted cal                     0
   Diffmode                        NOT_SPECIFIED
   Swing                           NOT_SPECIFIED
   rcvload_cal                     NOT_SPECIFIED
   cal_type                        NOT_SPECIFIED
   cal_pat                         99
   target_rise                     99
   target_fall                     99
   cal_freq                        99
   dut_voh                         99
   dut_vol                         99
   dut_rise_time                   99
   dut_fall_time                   99
```

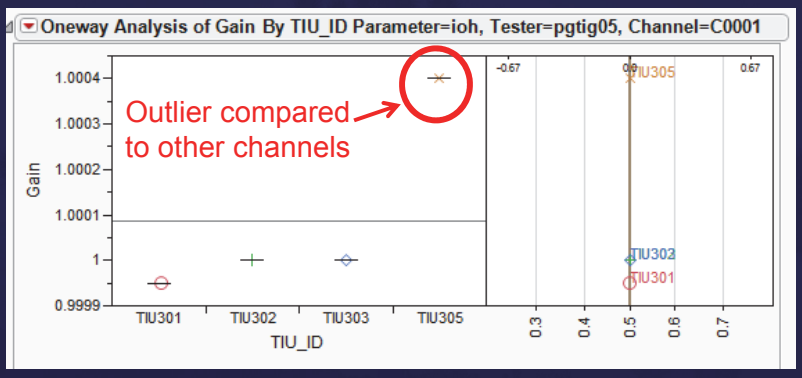
Raw calibration file converted to JMP readable files in order to proceed for data analysis.

	Tester	TIU_ID	Channel	Parameter	Gain	Offset
1	pgtig05	TIU301	C0001	vol	0.99496	0.017761
2	pgtig05	TIU301	C0001	voh	0.99603	0.011202
3	pgtig05	TIU301	C0001	iol	1.006	0.00013925
4	pgtig05	TIU301	C0001	ioh	0.99995	0.00032654
5	pgtig05	TIU301	C0001	vil	1.0043	-0.027669
6	pgtig05	TIU301	C0001	vih	1.0039	-0.022194
7	pgtig05	TIU301	C0002	vol	0.99576	0.0076058
8	pgtig05	TIU301	C0002	voh	0.99536	0.013923
9	pgtig05	TIU301	C0002	iol	1.0031	0.00026961
10	pgtig05	TIU301	C0002	ioh	0.99934	0.00026297
11	pgtig05	TIU301	C0002	vil	1.0048	-0.030337
12	pgtig05	TIU301	C0002	vih	1.0041	-0.021741
13	pgtig05	TIU301	C0003	vol	0.99516	0.0015038
14	pgtig05	TIU301	C0003	voh	0.99508	0.016096
15	pgtig05	TIU301	C0003	iol	1.0069	8.67E-05
16	pgtig05	TIU301	C0003	ioh	0.999	8.00E-05
17	pgtig05	TIU301	C0003	vil	1.0033	-0.030718
18	pgtig05	TIU301	C0003	vih	1.0046	-0.02113
19	pgtig05	TIU301	C0004	vol	0.9946	-0.0031533
20	pgtig05	TIU301	C0004	voh	0.99623	0.0046459
21	pgtig05	TIU301	C0004	iol	1.0073	1.04E-05
22	pgtig05	TIU301	C0004	ioh	1.0002	0.00012133
23	pgtig05	TIU301	C0004	vil	1.0042	-0.027624
24	pgtig05	TIU301	C0004	vih	1.0045	-0.023434

Results & Data Interpretation

Graphical Analysis Result

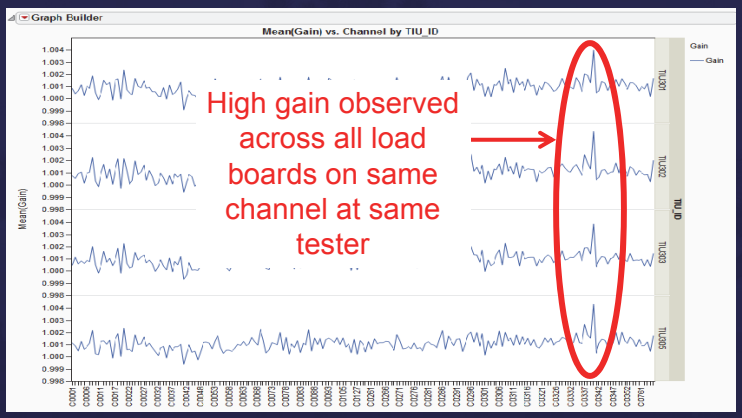
1). Detect channel performance differences between load boards.



Action: Troubleshoot problematic load board on the specific channel.

Graphical Analysis Result

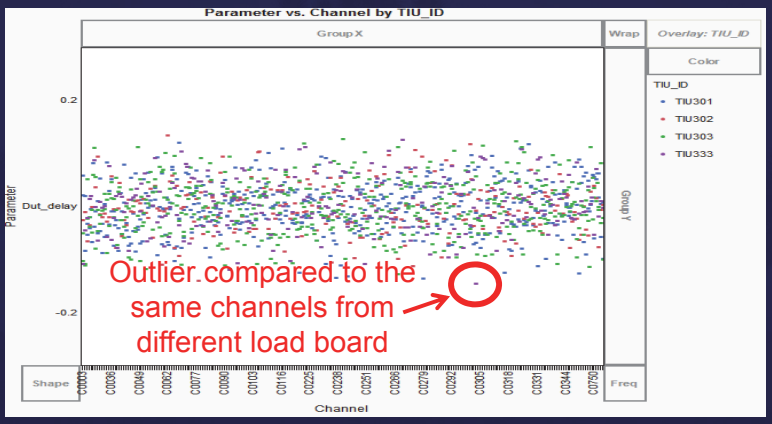
2). Detect tester marginal issue on specific channel



Action: Change tester pogo pin or marginal failing instrument board.

Graphical Analysis Result

3). Detect trace length differences on different load boards via TDR calibration data

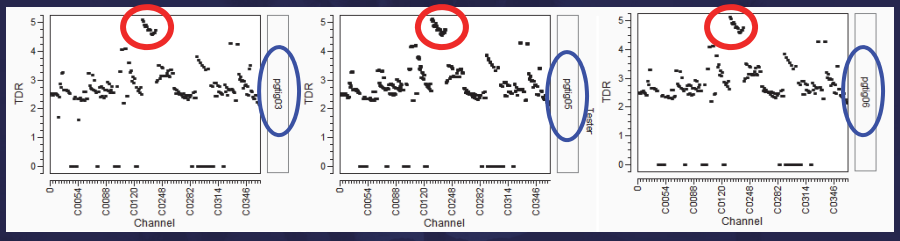


Action: Check load board Gerber file and ensure trace length compliance.

Graphical Analysis Result

4). Detect trace length design issue via TDR calibration data

Observed high TDR data shown across same channels at different testers



Action: Check load board Gerber file and ensure trace length compliance.

Project Summary

- Implementation of project is FAST & SIMPLE.
- Applicable to both Unix and Windows based ATE.
- Project Advantages:
  - Simplify data analysis task by using scheduler auto-scripts
  - Real time marginal tools monitoring
  - Detect marginal tools performance with reference to analyzed data
  - Detect load board design issue via TDR calibration data
  - Improve overall tool stability through early problem detection
- Improvement areas based on pilot assessment:
  - 15% unscheduled downtime improvement
  - 0.5% product yield improvement

Acknowledgement

- LT Yew (Test Engineering Manager)
- TS Yeoh (Principal Engineer)
- KC Cheng (Engineering GL)
- BK Lee (Yield Engineer)
- Katerine Goh (IT Engineer)